

TRENCH CAPACITOR AND METHOD FOR FABRICATING IT

5 Background of the Invention:

Field of the Invention:

The invention relates to a trench capacitor for storing an electrical charge and to a method for fabricating such a trench capacitor.

10 Integrated circuits (ICs) or chips contain capacitors for the purpose of storing electrical charges, such as, for example, in a dynamic random access memory (DRAM). The charge state in the capacitor represents a data bit in this case.

15 In order to maintain or increase international competitiveness, it is necessary to continually reduce the costs that have to be expended to realize a specific electronic function, and thus to continuously increase
20 productivity. The continuous increase in productivity is achieved by a progressive miniaturization. This necessitates realizing an ever greater number of functions on the same chip area. This is accompanied by a continuous reduction in the
25 dimensions of the capacitors used for charge storage are also reduced.

However, the progressive miniaturization of the capacitors entails a decrease in the capacitance of the capacitors. A series of applications, such as DRAM memories for example, require a minimum storage capacitance of the storage capacitors. Therefore, it is necessary to maintain or even to increase the storage capacitance of the storage capacitors despite reduced structural dimensions. If, as is generally customary nowadays, silicon oxide is used as a capacitor dielectric, then the layer thickness of the storage dielectric would have to be reduced to a few atomic layers in future technologies. However, it is very difficult to fabricate such thin silicon oxide layers reproducibly and with sufficient accuracy, because fluctuation in the layer thickness by one atomic layer means fluctuation by more than 10%. Furthermore, it is very difficult to adequately suppress the leakage currents between two capacitor electrodes which are isolated by a storage dielectric having a thickness of a few atomic layers, since, through the effect of quantum mechanical tunneling, the charge carriers can tunnel through the potential barrier produced by the thin storage dielectric.

The prior art has already disclosed capacitors in which the storage capacitance is increased using materials such as tantalum oxide (TaO_2) having a dielectric constant $\epsilon_r = 20$, and also barium strontium titanate (BST, $(\text{Ba}, \text{Sr}) \text{TiO}_3$) having an

ϵ_r of up to 1000 or lead zirconate titanate (PZT, Pb (Zr, Ti) O₃). However, complicated and costly deposition methods are necessary for the use of BST, PZT or SBT layers, and barrier layers made of platinum (Pt), ruthenium (Ru) or ruthenium oxide (RuO₂) that are difficult to process are also necessary.

The increase in the dielectric constant ϵ_r through the use of TaO₂ ($\epsilon_r = 20$) is relatively small in comparison with NO or ONO layers, which already have a dielectric constant of $\epsilon_r = 6$ to 8. Although the dielectric constant is significantly above that when BST, PZT or SBT is used, the capacitance of the capacitors is nonetheless limited by the required barrier layers with respect to silicon and polysilicon layers which serve as electrodes.

In the case of BST, PZT and SBT, it has been found that these materials belong to the materials which, chemically, cannot be etched or can be etched only with difficulty, in the case of which the etching removal, even given the use of reactive gases, is based predominantly or almost exclusively on the physical component of the etching. Due to the small or absent chemical component of the etching, the etching removal of the layer to be patterned is of the same order of magnitude as the etching removal of the mask or of the support (etching stop).

Therefore, the etching selectivity with respect to the etching

mask or with respect to the support is generally small, the consequence of which is that, due to the erosion of masks with inclined sidewalls and the unavoidable faceting (beveling, tapering) on the masks, only low dimensional accuracy of the patterning can be ensured. The faceting thus limits the smallest feature sizes that can be attained in the course of patterning, and also the attainable steepness of the profile sidewalls in the layers to be patterned.

Due to a lack of thermal stability, BST layers cannot, moreover, be used for processes which provide high-temperature steps after the formation of the BST layer, as is the case for example in the fabrication of DRAM memories with deep trench capacitors.

Summary of the Invention:

It is accordingly an object of the invention to provide a trench capacitor which overcomes the above-mentioned disadvantages of the heretofore-known trench capacitors of this general type and which provides a high storage capacitance in relation to its geometrical dimensions and has sufficient thermal stability for process steps which are carried out after its formation. It is a further object of the invention to provide a method of producing such a trench capacitor.

With the foregoing and other objects in view there is provided, in accordance with the invention, a trench capacitor, including:

5 a substrate formed with a trench;

the trench having an upper region and a lower region;

an insulation collar formed in the upper region;

10 a buried well formed in the substrate, the lower region at least partly extending through the buried well;

15 a dielectric layer of tungsten oxide for lining the lower region, the dielectric layer serving as a capacitor dielectric; and

a conductive trench filling disposed in the trench.

20 The idea underlying the invention is the use of tungsten oxide (WO_x) as a capacitor dielectric. Since tungsten oxide has dielectric constants ϵ_r of greater than 50 and even greater than 300, the capacitance of the trench capacitor is increased, whilst maintaining the geometrical dimensions, by
25 approximately 2 orders of magnitude (factor 100) if tungsten oxide is used instead of silicon oxide. The trench capacitor

according to the invention has the advantage, moreover, that the installations used in semiconductor technology can likewise be used for producing tungsten oxide layers.

Specially adapted and thus expensive installations, as are

5 required for fabricating BST, PZT or SBT layers, do not have to be used. The tungsten used for producing tungsten oxide layers diffuses only very slightly into silicon, resulting in a reduced risk of contamination in the case of the trench capacitor according to the invention. The use of tungsten

10 oxide as a capacitor dielectric is not restricted to silicon technology, however, but rather may also be used in connection with other semiconductors such as, for example, gallium

arsenide (GaAs). Tungsten oxide can be used as a capacitor dielectric outside the scope of semiconductor technology as

15 well, such as, for example, in discrete components for low-voltage and high-voltage technology. Furthermore, tungsten oxide has markedly good thermal stability up to temperatures in excess of 1100°C. As a result, tungsten oxide can be used as a storage dielectric in memory cells having a trench

20 capacitor, in which a transistor is formed after the trench capacitor has been fabricated, because the processing of a transistor requires, for example, thermal steps for annealing source and drain regions which are above 1000°C.

25 Progressive miniaturization additionally has the consequence that the sheet resistance of capacitor electrodes continuously

increases, due to the decreasing layer thickness. Therefore, in an advantageous embodiment, at least one of the capacitor electrodes is composed of tungsten or a tungsten-containing material. As a result, the resistance of the capacitor

5 electrodes is reduced and the time needed for charging and discharging the trench capacitor is advantageously shortened.

In accordance with another feature of the invention, the conductive trench filling is a tungsten-containing material.

10 In a further advantageous embodiment of the invention, the tungsten-containing material is composed of tungsten silicide, tungsten nitride or of pure tungsten.

15 In a further advantageous embodiment of the invention, the dielectric layer forming the capacitor dielectric has a dielectric constant $\epsilon_r > 50$.

20 In accordance with another feature of the invention, a barrier layer is disposed between the dielectric layer and the substrate and/or between the dielectric layer and the conductive trench filling.

25 In a further advantageous embodiment of the invention, a barrier layer made of silicon oxide, silicon nitride, oxynitride, tungsten nitride, titanium nitride or tantalum

nitride is formed, which is situated between the tungsten oxide layer, which forms the capacitor dielectric, and the buried plate of the capacitor, which is composed of doped silicon.

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In a further advantageous embodiment of the invention, a vertical transistor is additionally situated in the trench, and serves as a selection transistor for the memory cell.

10 With the objects of the invention in view there is also provided, a method of producing a trench capacitor, the method includes the steps of:

introducing a buried well into a substrate;

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forming a trench in the substrate, the trench having an upper region and a lower region;

forming an insulation collar in the upper region;

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providing a capacitor dielectric by forming a dielectric layer of tungsten oxide lining the lower region; and

filling the trench with a conductive trench filling for

25 providing an inner capacitor electrode.

In an advantageous fabrication method, the dielectric layer is formed by the deposition of a tungsten-containing layer, which is subsequently thermally oxidized in an oxygen-containing atmosphere.

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In accordance with another mode of the invention, the tungsten-containing layer is formed from tungsten nitride, tungsten silicide or pure tungsten.

10 In a further advantageous embodiment of the method according to the invention, the oxidation of the tungsten-containing layer is carried out at a temperature from 200°C to 600°C in an oxygen-containing atmosphere, a water-containing atmosphere, an N₂O-containing atmosphere and/or an NO-
15 containing atmosphere.

A further advantageous fabrication method forms the dielectric layer by reactive sputtering of tungsten in an oxygen-containing atmosphere. In this case, tungsten is converted
20 into tungsten oxide before the dielectric layer is formed.

A further advantageous embodiment of the fabrication method according to the invention carries out a thermal treatment of the dielectric layer at temperatures of between 550 and
25 1100°C, with the result that the dielectric layer composed of tungsten oxide develops a dielectric constant $\epsilon_r > 50$.

In a further advantageous fabrication method, the tungsten-containing material of which the conductive trench filling is composed or from which a tungsten-containing layer is formed
5 is fabricated by a CVD (Chemical Vapor Deposition) method. Furthermore, the CVD method may involve a selective CVD deposition in which tungsten is deposited selectively with respect to silicon oxide and silicon nitride on silicon. The selective CVD deposition may be carried out for example using
10 tungsten hexafluoride (WF_6) as a starting material at temperatures from 200 to 600°C.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

15 Although the invention is illustrated and described herein as embodied in a trench capacitor for charge storage and a method for fabricating it, it is nevertheless not intended to be limited to the details shown, since various modifications and
20 structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention,
25 however, together with additional objects and advantages thereof will be best understood from the following description

of specific embodiments when read in connection with the accompanying drawings.

Brief Description of the Drawings:

- 5 Fig. 1 is a diagrammatic, partial sectional view of an exemplary embodiment of a trench capacitor according to the invention, corresponding to a first embodiment of the method according to the invention;
- 10 Fig. 2 is a diagrammatic, partial sectional view of a further exemplary embodiment of a trench capacitor according to the invention, corresponding to a second embodiment of the method according to the invention;
- 15 Fig. 3a is a diagrammatic, partial sectional view of a further exemplary embodiment of a trench capacitor according to the invention, corresponding to a further embodiment of the method according to the invention;
- 20 Fig. 3b is a diagrammatic, partial sectional view of a further exemplary embodiment of a trench capacitor according to the invention, corresponding to a further embodiment of the method according to the invention;
- 25 Fig. 4 is a diagrammatic, partial sectional view of a further exemplary embodiment of a trench capacitor according to the

invention, corresponding to a further embodiment of the method according to the invention;

Fig. 5 is a diagrammatic, partial sectional view of a trench capacitor configuration illustrating an embodiment of the method for fabricating a trench capacitor according to one of Figs. 1 to 4;

Fig. 6 is a diagrammatic, partial sectional view of a further embodiment of a trench capacitor configuration for the fabrication of a trench capacitor according to the invention as shown in Fig. 1 or 4;

Fig. 7 is a diagrammatic, partial sectional view of a further embodiment of a trench capacitor configuration for the fabrication of a trench capacitor according to the invention as shown in Fig. 2;

Fig. 8 is a diagrammatic, partial sectional view of a further embodiment of a trench capacitor configuration for the fabrication of a trench capacitor according to the invention as shown in Fig. 3a; and

Fig. 9 is a diagrammatic, partial sectional view of a further embodiment of a trench capacitor configuration for the

fabrication of a trench capacitor according to the invention as shown in Fig. 3a.

Description of the Preferred Embodiments:

5 In the figures, identical reference symbols designate identical or functionally identical elements. Referring now to the figures of the drawings in detail and first, particularly, to Fig. 1 thereof, there is shown a first embodiment of the invention. The memory cell 100 illustrated
10 includes a trench capacitor 160 and a transistor 110. The trench capacitor 160 is formed in a substrate 101. A buried well 170, which is composed of a dopant material for example, is introduced in the substrate 101. The trench capacitor 160 has a trench 108 having an upper region 109 and a lower region
15 111. An insulation collar 168 is situated in the upper region 109 of the trench 108. The lower region of the trench penetrates at least partially through the buried well 170. Provided around the lower region 111 of the trench 108 is a buried plate 165, which forms the outer capacitor electrode.
20 The buried plates 165 of the adjacent memory cells are electrically connected to one another by the buried well 170.

The lower region 111 of the trench 108 is lined with a dielectric layer 164, which forms the storage dielectric of
25 the trench capacitor 160. According to the invention, the dielectric layer 164 is composed of tungsten oxide.

The trench 108 is filled with a conductive trench filling 161, which forms the inner capacitor electrode of the trench capacitor 164.

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The transistor 110 includes a source region 114 and a drain region 113, which is connected to an edgeless contact 183. Furthermore, the transistor 110 includes a channel 117 controlled by a gate 112. The gate 112 is connected to a word line 120. The edgeless contact 183 is connected to a bit line 185 running above a dielectric layer 189.

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Situated above the conductive trench filling 161 is a conductive buried bridge or strap 162, which is connected to the source region 114 of the transistor 110 with the aid of a buried contact 250.

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In this variant, a passing word line 120' runs above a trench insulation 180, the word line being insulated from the trench filling 161 by the trench insulation 180.

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Fig. 2 shows a further embodiment of the trench capacitor 160 according to the invention, which differs from the variant illustrated in Fig. 1 by the fact that the dielectric layer 164 is not limited to the lower region 111 of the trench 108, rather the dielectric layer 164 is additionally situated in

the upper region 109 of the trench 108 on the insulation collar 168.

Fig. 3a illustrates a further embodiment of the trench capacitor according to the invention. The variant of the trench capacitor 160 that is illustrated in Fig. 3a differs from the variant illustrated in Fig. 2 by virtue of an additional barrier layer 167, which is situated in the trench 108 between the dielectric layer 164 and the buried plate 165 and between the dielectric layer 164 and the insulation collar 168, respectively.

Fig. 3b illustrates a variant of the trench capacitor 160 shown in Fig. 3a. Fig. 3b differs from Fig. 3a by virtue of an oxide region 167', which is provided in case a conductive barrier layer 167 is used. The oxide region 167' has the purpose of providing insulation between the conductive trench filling 161 and the barrier layer 167 and is disposed between the insulation collar 168, the dielectric layer 164, the barrier layer 167 and the conductive buried bridge 162.

Fig. 4 shows a further variant of the trench capacitor 160 according to the invention, which differs from the variant shown in Fig. 1 by the fact that a vertical transistor 220 is provided in the trench 108 above the insulation collar 168.

With reference to Fig. 5, a substrate 101 is provided for the fabrication of the trench capacitor 160 according to the invention. In the present variant, the substrate 101 is composed of silicon and is lightly doped with p-type dopants, such as boron for example. An n-doped buried well 170 is formed at a suitable depth in the substrate 101. Phosphorous or arsenic can be used as the dopant for doping the buried well 170. The buried well 170 may be produced by implantation for example. It serves for insulating the p-type well from the substrate 101 and additionally forms a conductive connection between the buried plates 165 of the adjacent trench capacitors. As an alternative, the buried well 170 may be formed by epitaxially grown, doped silicon layers, or by a combination of crystal growth (epitaxy) and implantation. This technique is described in U.S. Patent No. 5,250,829 to Bronner et al.

A layer stack is formed on the surface of the substrate 101 and includes, by way of example, a substructure oxide layer 104 and a substructure stop layer 105, which can be used as polish or etching stop and is composed of nitride for example. A hard mask layer 106 may optionally be provided above the substructure stop layer 105. The hard mask layer may be composed of tetraethyl orthosilicate (TEOS) or other materials such as, for example, borosilicate glass (BSG). In addition,

an antireflection coating (ARC) can be used in order to improve the lithographic resolution.

The hard mask layer 106 is patterned using customary photolithographic techniques, in order to define a region 102 in which the trench 108 is to be formed. The hard mask layer 106 is subsequently used as an etching mask for a reactive ion etching step which forms the deep trench 108.

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10 A natural oxide layer is formed in the trench 108, and serves as an etching stop in subsequent etching steps. The trench is subsequently filled with an insulation collar sacrificial layer 152, which ensures sufficient thermal stability up to 1100°C and can be removed selectively with respect to nitride
15 and/or oxide, such as, for example, polysilicon, amorphous silicon or other suitable materials. In this process variant, the insulation collar sacrificial layer 152 is composed of polysilicon. The polysilicon sacrificial layer is sunk in the trench 108 down to the underside of the insulation collar 168
20 to be formed. The removal of the sacrificial layer may be carried out, by way of example, by planarization through the use of chemical mechanical polishing (CMP) or chemical dry etching (CDE) or selective ion etching. The insulation collar sacrificial layer 152 is then sunk in the trench 108 by
25 selective ion etching. The use of chemical dry etching to sink

the insulation collar sacrificial layer in the trench 108 is likewise possible.

A dielectric layer is subsequently deposited on the wafer, and covers the layer stack and the sidewalls of the trench 108 in its upper region 109. The dielectric layer is used to form the insulation collar 168 and is composed of oxide for example. The dielectric layer is subsequently etched, for example by reactive ion etching (RIE) or through the use of CDE, in order to form the insulation collar 168. The chemical agents for the reactive ion etching are chosen in such a way that the oxide of the insulation collar 168 is etched selectively with respect to the polysilicon of the insulation collar sacrificial layer 152 and the nitride of the hard mask layer 106.

The insulation collar sacrificial layer 152 is subsequently removed from the lower region of the trench 108. This is preferably achieved by CDE etching, the thin natural oxide layer serving as a CDE etching stop. As an alternative, wet etching, for example using KOH or HF-NHO₃ and CH₃OOH mixture, can likewise be used during the removal of the insulation collar sacrificial layer 152. After the removal of the insulation collar sacrificial layer 152, the thin natural oxide layer is removed through the use of etching vapor and a buried plate 165 with n-type dopant, such as arsenic or

phosphorus for example, is formed as the outer capacitor electrode. In this case, the insulation collar 168 serves as a doping mask which limits the doping to the lower region 111 of the trench 108. In order to form the buried plate 165, it is possible to use vapor phase doping, plasma doping or plasma immersion ion implantation (PII). These techniques are described for example in Ransom et al., J. Electrochemical. SOC., Vol. 141, No. 5 (1994), p. 1378 ff.; U.S. Patent No. 5,344,381 and U.S. Patent No. 4,937,205. Ion implantation using the insulation collar 168 as a doping mask is likewise possible. As an alternative, the buried plate 165 can be formed using a doped silicate glass, such as ASG for example, as dopant source. This variant is described for example in Becker et al., J. Electrochemical. SOC., Vol. 136 (1989), p. 3033 ff. If doped silicate glass is used for the doping, then it is removed after the formation of the buried plate 165.

With reference to Fig. 6, a dielectric layer 164 composed of tungsten oxide is formed. In order to form the tungsten oxide layer, a tungsten layer, for example, may be deposited which is subsequently oxidized. In order to deposit the tungsten layer, selective tungsten deposition, for example, is used, which forms a tungsten seed layer in the lower region 111 of the trench 108 on the uncovered silicon areas. The tungsten seed layer may be formed using a CVD process, for example,

which grows WF_6+SiH_4 at 500 Pa and 470°C. The tungsten seed layer forms selectively on the uncovered silicon surfaces. In a second step, the tungsten bulk layer is grown, which is formed using a CVD process with the starting substances WF_6+H_2 at 10^4 Pa and 470°C. In this case, the tungsten bulk layer is formed selectively on the tungsten seed layer. During a subsequent oxidation process, the tungsten layer that has been formed is oxidized and a tungsten oxide layer is produced, which constitutes the dielectric layer 164.

In the subsequent process step, the conductive trench filling 161 is formed. To that end, using a CVD method for example, a doped, amorphous silicon is deposited into the trench 108 and onto the substrate surface. The conductive trench filling 161 may also be formed from tungsten, tungsten nitride or tungsten silicide. If the conductive trench filling 161 is formed from tungsten, then it is possible to use a CVD process with the starting substances WF_6+H_2 at 10^4 Pa and 470°C. In order to fabricate the conductive trench filling 161 from tungsten nitride, it is possible, for example, to produce a tungsten layer by the method mentioned above. The layer is then thermally nitrified. In this case, it is also possible to effect the alternately stepwise deposition of thin tungsten layers and nitrifying of these thin tungsten layers until the entire conductive trench filling 161 has been formed from tungsten nitride. As an alternative, tungsten nitride can be

formed using a CVD tungsten nitride method which, from
4 $\text{WF}_6 + \text{N}_2 + 12\text{H}_2$, forms the desired 4 $\text{W}_2\text{N} + 24 (\text{HF})$ at 350 to
400°C. If the conductive trench filling 161 is formed from
tungsten silicide, then it is possible to use a CVD method
5 with the starting substances $\text{WF}_6 + \text{SiH}_2\text{Cl}_2$.

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10 The method for fabricating a trench capacitor in accordance
with Fig. 3a is described with reference to Fig. 7. The
process steps as were explained in connection with Fig. 5 are
carried out for this purpose. Following the process stage
shown in Fig. 5, the dielectric layer 164 is formed from
tungsten oxide. In contrast to the fabrication method shown in
Fig. 6, in Fig. 7 the dielectric layer is formed not only in
the lower region 111 of the trench 108 but also in the upper
15 region 109 of the trench 108, in which the insulation collar
168 is situated. In order to form the tungsten oxide layer, a
tungsten layer, for example, may be deposited which is
subsequently oxidized. In order to form the tungsten layer,
selective tungsten deposition is not used in this case but
20 rather, by way of example, a CVD tungsten deposition process
which uses the starting substances $\text{WF}_6 + \text{H}_2$ at 470°C and 10^4 Pa
in order to form a tungsten layer. During a subsequent
oxidation process, the tungsten layer that has been formed is
oxidized and a tungsten oxide layer is produced, which forms
25 the dielectric layer 164.

The conductive trench filling 161 is formed in the subsequent process step, as has already been described in connection with Fig. 6.

5 Fig. 8 illustrates a method for fabricating a trench capacitor in accordance with Fig. 3a. Following the process stage from Fig. 5, firstly a barrier layer 167 is formed in the trench 108. The barrier layer 167 is composed of tungsten nitride for example. In order to form the barrier layer 167 from tungsten
10 nitride, a tungsten layer, for example, may be deposited in the trench 108. The layer is then nitrided. The abovementioned CVD tungsten deposition processes are suitable for depositing a tungsten layer. The deposited tungsten layer is nitrided in a further process step under a nitrogen atmosphere. A further
15 method for producing a tungsten nitride layer is the direct CVD deposition of a tungsten nitride layer. To that end, it is possible to use, for example, a CVD method with the starting materials $4 \text{ WF}_6 + \text{N}_2 + 12\text{H}_2$ at a temperature of from 350 to 400°C. The layer thickness of the tungsten nitride layer thus
20 produced can be produced in a range of from a few nanometers to several micrometers. In the subsequent process step, the dielectric layer 164 is formed from tungsten oxide. To that end, a tungsten layer is deposited by a CVD method and is converted into tungsten oxide in a subsequent oxidation
25 process. A further method for fabricating the barrier layer 167 and the dielectric layer 164 includes the deposition of a

tungsten layer with the aid of a CVD tungsten deposition method. The tungsten layer is then thermally nitrided to form the barrier layer 167. In a further thermal process, the barrier layer 167 that has been formed is oxidized, with the result that part of the barrier layer 167 is converted into the dielectric layer 164 composed of tungsten oxide. The conductive trench filling 161 is formed in the manner described in connection with Fig. 6.

10 A variant of the method according to the invention in which the barrier layer is formed from a conductive material will now be described with reference to Fig. 3b. After the sinking of the conductive trench filling 161, the dielectric layer 164 and the barrier layer 167 in the trench 108, a thermal
15 oxidation is carried out. In this case, the conductive material of which the barrier layer 167 is composed is oxidized locally on its uncovered surface, thereby producing the insulating oxide region 167'. Examples of materials that may be used for the conductive barrier are tungsten nitride,
20 titanium nitride and/or tantalum nitride, which are converted by the oxidation into tungsten oxide, titanium oxide and tantalum oxide, respectively. Since the conductive trench filling 161 also oxidizes on its surface, this oxide layer is removed through the use of buffered HF or dilute HF
25 selectively with respect to the oxide region 167'.

A further exemplary embodiment of the invention is illustrated in Fig. 9. In this configuration, a further barrier layer 167'' is situated between the dielectric layer 164 and the conductive trench filling 161. The further barrier layer 167'' forms a controlled interface between the dielectric layer 164 and the conductive trench filling 161, thereby preventing the formation of small holes (wormholes) in the interface. Furthermore, the effective dielectric constant of the trench capacitor is increased since the further barrier layer 167'' is formed in a well-defined and controlled manner. In addition, the further barrier layer 167'' prevents the diffusion of material and thus the mixing of conductive trench filling 161 and dielectric layer 164. The further barrier layer 167'' may be formed for example from silicon nitride, silicon oxide or silicon oxynitride. Furthermore, it is also possible to use conductive materials such as tungsten nitride and/or titanium nitride for forming the further barrier layer 167''.

One method for fabricating the further barrier layer 167'' forms the further barrier layer after the formation of the dielectric layer 164. To that end, in a CVD process, for example, a silicon layer is deposited and reoxidized and/or renitrided. Another variant of the method provides a CVD deposition of a metal layer made of titanium, or tungsten. The

metal layer is then nitrided in a nitrogen-containing atmosphere through the use of a thermal step.

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